circuit, and said subtractor circuit subtracts the output of said second multiplier circuit from the output of said first multiplier circuit.

15. (Cancelled)

REMARKS

Claims 1-10, 12 and 14 are now pending in this application. Claims 11, 13 and 15 have been cancelled without prejudice or disclaimer of the subject matter thereof. The allowance of claims 1, 2, 6 and 7 is acknowledged with appreciation. Reconsideration of this application is requested.

The rejection of claim 8 as being anticipated by Reed et al., U.S. Patent No. 6,493,163 is respectfully traversed. According to the invention as set forth in claim 8, a phase detector circuit includes a combination of at least one multiplier circuit and a subtractor circuit, which combination performs an arithmetic operation on only the input random NRZ signal, the delayed signal, and the second signal related to the input random NRZ signal, as taught in Figs. 1, 2, 4, 6, 7, 9 and 11. As is generally accepted by those skilled in the art, an arithmetic operation includes the four basic operations of arithmetic, i.e., addition, subtraction, multiplication or division, but does not include a delay operation.

In contrast, Reed discloses in Fig. 2 a first multiplier 230 that multiplies a delayed input signal y1 with a binary slice signal s0, a second multiplier 231 that multiplies a delayed slice signal s1 with the input signal y0, and a subtractor 240 that subtracts the product of multiplier 231 from the product of multiplier 230. The combination of multipliers 230, 231 and subtractor 240 does not arithmetically operate on only an input signal, a delayed signal, and a second signal related to the input signal, as set forth in claim 8. Accordingly, Reed does not anticipate the invention set forth in claim 8 and this ground of rejection should be withdrawn.

The rejection of claims 9 and 10 as being obvious over Reed, and the rejection of claim 11 as being obvious over Reed in view of Iinuma and claim 12 as being obvious over Reed in view of Bhagwan, also are in error. The slice signal of Reed clearly is not the same as the input signal but differing in phase therefrom, but instead is simply a binary output of 1, 0, or -1 as a result of comparison of the input signal with a

predetermined threshold. Further, neither the Iinuma patent nor the Bhagwan patent suggest modifying Reed Fig. 2 to include a voltage-controlled delay circuit or a latch.

Similarly, the rejection of claim 14 is in error. Claim 14 requires a first multiplier for multiplying the input random NRZ signal with the second signal, and a second multiplier for multiplying the second signal with the output of the delay circuit. In contrast, in Fig. 2 of Reed multiplier 230 multiplies the delayed input signal with the slice signal s0, while the second multiplier 231 multiplies the input signal with a delayed slice signal s1. The multiplier 231 does not multiply the input signal with the second signal as alleged by the Examiner. It is improper for the Examiner to equate the delayed slice signal s1 with the slice signal s0 as if they were the same.

Because claim 8 is generic to claims 3, 4, and 5, and claim 8 is submitted to be patentably distinguishable over the prior art of record, the Examiner should now consider claims 3, 4 and 5 on the merits as the subject matter of these claims are specific instances of the invention recited in claim 8 and are encompassed by claim 8. As such, claims 3, 4 and 5 should be allowed if the Examiner agrees that claim 8 is allowable as discussed above.

In conclusion, further and favorable reconsideration of this application, withdrawal of the outstanding grounds of rejection, and the issuance of a Notice of Allowance are earnestly solicited.

Please charge any fee or credit any overpayment pursuant to 37 CFR 1.16 or 1.17 to Deposit Account No. 02-2135.

RESPECTFULLY SUBMITTED,			
NAME AND REG. NUMBER	Vincent M. DeLuca Attorney for Applicants Registration No. 32,408		
SIGNATURE	Vincent M DeLuca	DATE	30 OCT 03

Address	Rothwell, Figg, Ernst & Manbeck 1425 K Street, N.W., Suite 800				
City	Washington	*State*	D.C.	*Zip Code*	20005
Country	U.S.A.	*Telephone*	202-783-6040	*Fax*	202-783-6031